

Method of Forming a Source/Drain and a Transistor Employing the Same

ABSTRACT OF THE DISCLOSURE

A method of forming a source/drain having a reduced junction capacitance and a transistor employing the same. In one embodiment, the method of forming the source/drain includes forming a recess in a substrate adjacent a gate of the transistor and forming a deep doped region below a bottom surface of the recess. The method also includes epitaxially growing a semiconductor material within the recess and forming a lightly doped drain region adjacent the gate.